REMARKS

Claims 1-24 are pending in this application. By this Amendment, claims 16-24 are added.

The Office Action rejects claims 1-15 under 35 U.S.C. §102(e) by U.S. Patent 6,401,200 to Nishiike et al. (hereafter Nishiike). The rejection is respectfully traversed.

Independent claim 1 recites requesting an information down-load from the lower processors to the upper processor, accessing a memory of the upper processor containing the requested information down-load, grouping the lower processors with a representative address and creating the accessed information in an IPC format and transferring the IPC format information by using the group representative address.

Nishiike does not teach or suggest all of the features of independent claim 1. In particular, Nishiike does not suggest grouping the lower processors with a representative address and creating the accessed information in an IPC format and transferring the IPC format information by using the group representative address. In addressing these features, the Office Action cites Nishiike's column 2, lines 55-67 and Figure 4. However, this does not teach or suggest these features. In particular, the disclosure provided at column 2, lines 57-67 is a "Summary of the Invention" section and includes a "high level" discussion. This disclosure in no way suggests grouping lower processors with a representative address and creating the accessed information in an IPC format and transferring the IPC format information by using the group representative address.

The Office Action appears to rely on the "common boot address" shown in Figure 5 for the claimed grouping the lower processors with a representative address. See Nishiike's to column 5, lines 1-39 for the discussion related to this Figure. This section clearly describes a boot process in which an address generator 220 generates an address that is supplied to various ones of the selectors 141, 142 and 143 and the master ROM 230. Data stored in the area of the master ROM 230 specified by the address may be written into the instruction memories 131, 132, and 133. The controller 200 may generate boot permission signals to the DSPs 111, 112, and 113, and the DSPs 111, 112, and 113 may read the download information stored in the respective instruction memories 131, 132, and 133 and store the read download information therein. The respective DSPs 111, 112, and 113 may send boot complete signals to the controller 200. There is no suggestion of grouping of the lower processors with a representative address as recited in independent claim 1. Rather, Nishiike teaches that specific selectors 141, 142 and 143 are used to correspond to each of the DSPs 111, 112 and 113. This does not relate to grouping the lower processors with a representative address.

Furthermore, Nishiike does not teach or suggest creating the accessed information in an IPC format and transferring the IPC format information by using the group representative address. The Office Action's citation to Nishiike's column 2, lines 55-67 in no way suggests an IPC format or transferring the IPC format information by using the group representative address. Rather, this section of Nishiike merely shows that if one DSP is receiving download information from a corresponding instruction memory, then a second DSP may receive

download information from a second corresponding instruction memory. As such, Nishiike does not teach or suggest all of the features of independent claim 1.

Nishiike does not teach or suggest all of the features of independent claim 10 and 16. That is, independent claim 10 recite grouping the second processors using a prescribed processor address and assembling the accessed information in a prescribed format and transferring the assembled requested information to at least two second processors using a group representative address. For at least similar reasons as set forth above, Nishiike does not teach or suggest these features.

Furthermore, independent claim 16 recites grouping a plurality of second processors using a representative address of the plurality of second processors, providing the requested information in an information processing code (IPC) format, and transferring the requested information in the IPC format based on the representative address of the plurality of second processors. For at least similar reasons as set forth above, Nishiike does not teach or suggest these features.

Accordingly, each of independent claims 1, 10 and 16 defines patentable subject matter. Claims 2-9 depend from claim 1, claims 11-15 depend from claim 10 and claims 17-24 depend from claim 16 and therefore define patentable subject matter at least for this reason. In addition, the dependent claims also recite features that further and independently distinguish over the applied references. For example, dependent claim 6 recites that group information is used to determine the group representative address, and wherein the group information comprises a

node address (NA), a BHIU address (BA), a cinu address (CA), and a slot address (SA). See also dependent claim 21. Nishiike in no way teaches or suggests the node address, BHIU address, cinu address and slot address. The Office Action merely asserts that these features are used in mobile communications. Nishiike also does not teach or suggest these features in combination with the other features of independent claim 1. Thus, dependent claim 6 (and similarly dependent claim 21) defines patentable subject matter at least for this additional reason.

Dependent claim 7 recites that the group representative address is set by using the CA and the SA among the group information. See also dependent claim 22. In addressing these features, the Office Action merely relies on Nishiike's column 1, lines 25-30. However, this section does not teach or suggest these features.

Dependent claim 8 recites grouping of the group representative address is responsive to one of only the CA among the group information, only the SA among the group information and both the CA and the SA among the group information. See also dependent claim 23. The Office Action again cites Nishiike's column 1, lines 25-30, which do not relate to these features.

Furthermore, dependent claim 9 recites that the IPC format information is concurrently transferred to all the lower processors using the group representative address. See also dependent claim 23. The Office Action cites Nishiike's Figure 4 to show these features. However, Nishiike does not teach concurrently transferring the IPC information format to all the lower processors using the group representative address. That is, Figure 4 does not suggest these features.

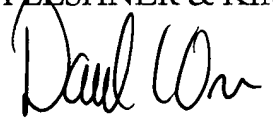
For at least these reasons, each of these dependent claims defines patentable subject matter. Withdrawal of the outstanding rejections is respectfully requested.

CONCLUSION

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-24 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **David C. Oren,** at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



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